Quality and Reliability Report 1st half 1995

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Detailed Test Results per Process and per Package type provided in the document Q&R 1st half 95 - Appendix supplied upon request.

1 Quality and Reliability Targets

The present report shows the results of the qualification and monitoring activities carried out in the 1st half of 1995.
The quality targets for 1995 are summarized hereafter, with the corresponding sampling rules and the measurements performed so as to check product and package quality and reliabilty.

1.1 Electrical Average Outgoing Quality

Target	10 ppm (Average value in Q4-95).
Sampling	125 parts (AQL 0.1%)or 200 parts (AQL 0.065%), every lot
Test	Quality control test programs.
Conditions	Each test temperature.

1.2 Early Failure Rate

Target	5 ppm / mm^2 (Average value in H2-95).
Sampling	2000 parts every 6 months.
Test	12 hours, Dynamic Life test.
Conditions	150°C - 5.75V.

1.3 Latent Failure Rate

Target	0.35 fit / mm^2 (Average value in H2-95). (UCL = 60%, Ea = 0.6 eV, Ta = 55°C)
Sampling	300 parts every 6 months.
Test	500 hours, Dynamic Life test.
Conditions	150°C - 5.75V.

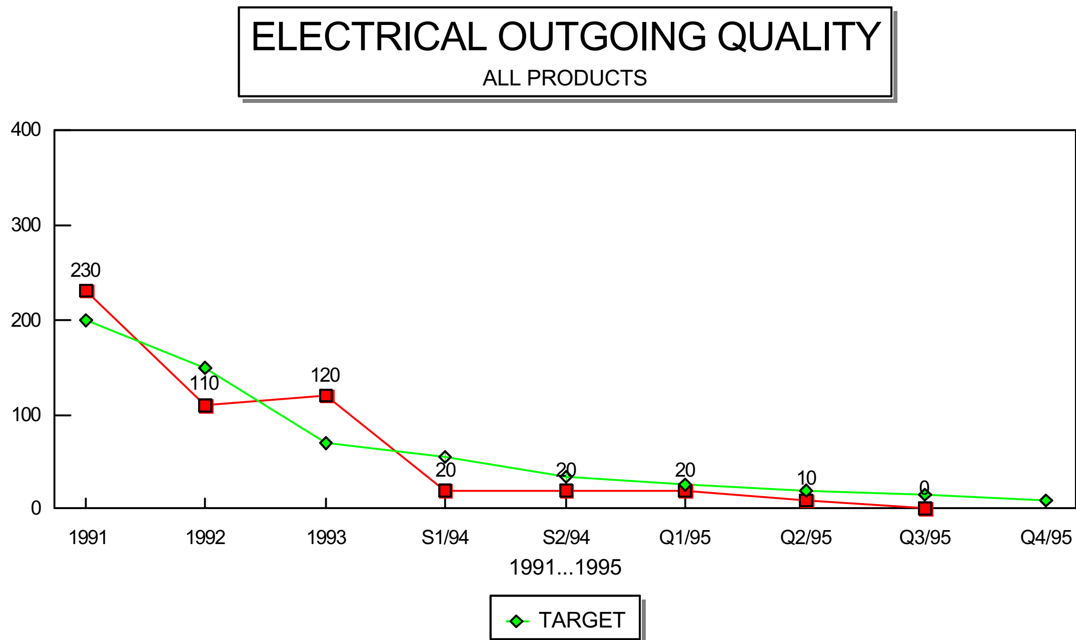
1.4 Climatic tests

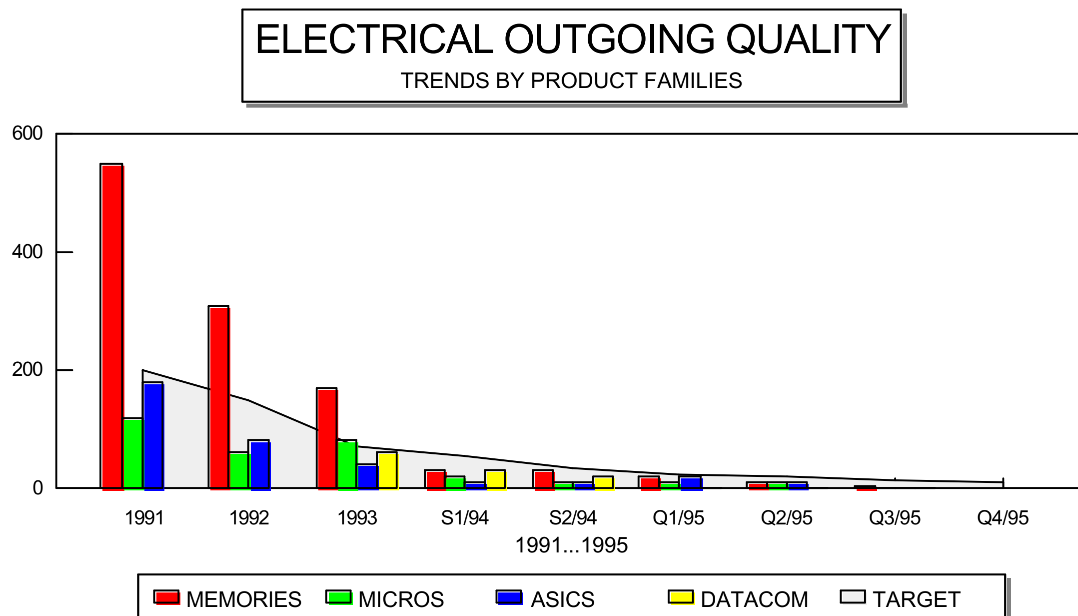
Temperature cycling	LTPD = 5.
Sampling	300 parts every 6 months.
Test	1000 cycles.
Conditions	Air / air, -65°C / +150°C or method 1010 cond C of MIL883.

Humidity	LTPD = 5.
Sampling	300 parts every 6 months.
Test	1000 hours in 85/85 or 168 hours in HAST.
Conditions	85°C/85%RH - 5.5 V or 130°C/85%RH - 5.5V

2 Overview of Quality and Reliability Data

2.1 Electrical Average Outgoing Quality (ppm)





2.2 Global Reliability Data

TESTS	SAMPLE SIZE	RESULTS
Early Failure Rate	161, 489 parts	700 ppm
EFR / mm2		25.3 ppm / mm2
Latent Failure Rate	9, 543, 892 test hrs	37.2 fits
LFR / mm2		1.29 fit / mm2
Temperature Cycles	4, 171 devices	0.36 %
Temp. Cycl. fail. rate	8.6 10^9 eq. dev. hrs	1.74 fits
Relative Humidity	5, 966 devices	0.15 %
Rel. Hum. fail. rate	13.6 10^9 eq. dev. hrs	0.66 fits

The measurement results of the Early Failure rate and of the Latent Failure rate are dependent on the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

As shown in page 2, the targets were previously settled for the overall range of products. Since 1994 the targets are settled for both EFR and LFR rated to 1 mm2.

Basic Definitions and Reliability Models:

The Early failure rate is defined as the failure rate observed within the first 24 hours life test at 140°C --5.5 V or 12 hours life test at 150°C --5.75V.

The Latent failure rate is determined using the Arrhenius equation with :
accel. factor = exp (E_a / K [1/T_{use} - 1/T_{stress}]) at Ta=55°C
and is derived from 500 hours or 1000 hours life test at 150°C - 5.75V with a confidence level of 60% and an average activation energy of 0.6 eV.

The Temperature cycling failure rate is determined using the Manson-Coffin equation with :
accel. factor = 0.5 $(G / 2E)^{1/c}$

where
G is the cyclic shear strain, G = n (Delta T) ^{Z}
E is the fatigue ductility,
c is the factile ductility exponent,
Delta T is the difference of temperature per cycle,
n and z are constants:
z = 3.415
n = 3.903 10^{-10}
c = -0.673 (usually between -0.7 and -0.5)
E = 3.09

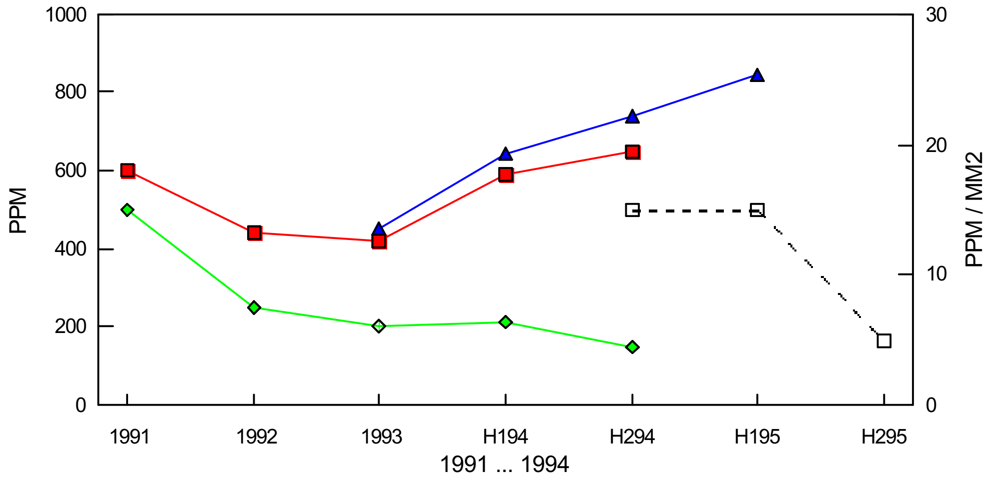
these parameters being determined for gold wire fatigue, and with the assumption of 3 temperature cycles per day between 0°C and 70°C (commercial range).

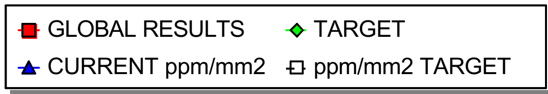
The Relative Humidity failure rate is determined from the Peck model with :
accel. factor = (RH_{stress} / RH_{use})$^{2.5}$ * exp (0.81 / k [1/T_{use} - 1/T_{stress}])

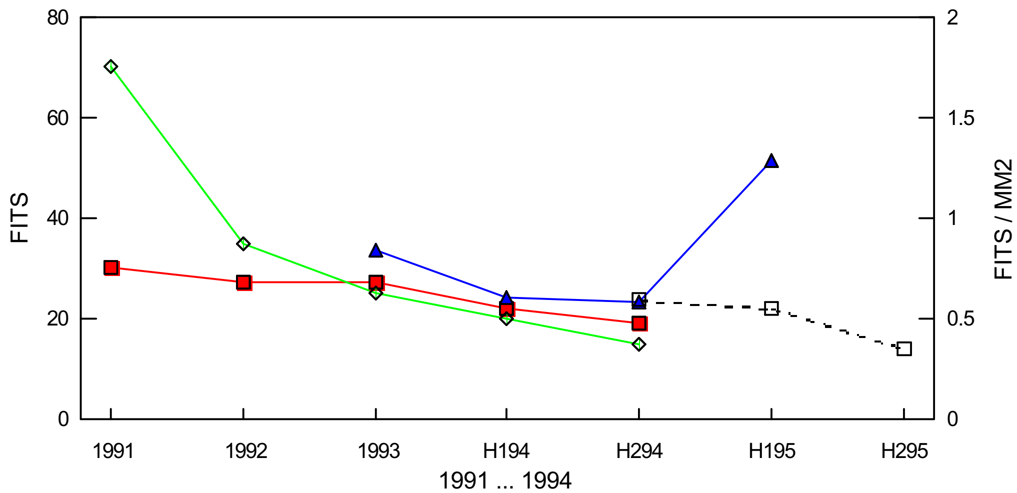
where RH_{use} is calculated at a device room temperature of 30°C and a room relative humidity of 60%. With a device junction temperature of 55°C, the relative junction humidity is then RH_{use} = 16.2%.
RH_{stress} depends on the stress condition, 85% or 100%.

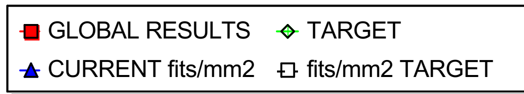
For the both climatic tests, the failure rate is calculated by dividing the number of fails by the number of the calculated equivalent device hours.

Global Reliability Data (cont'd)

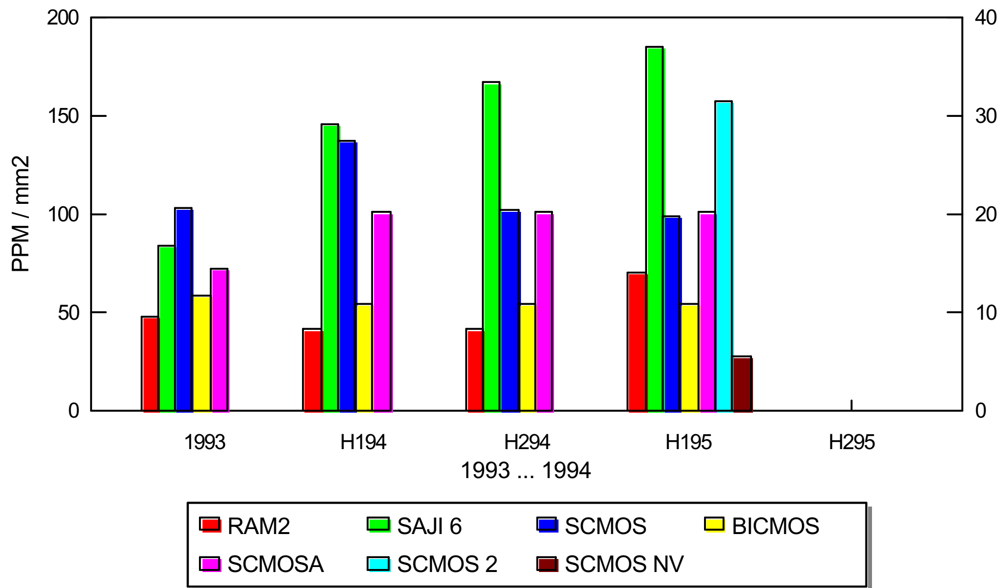


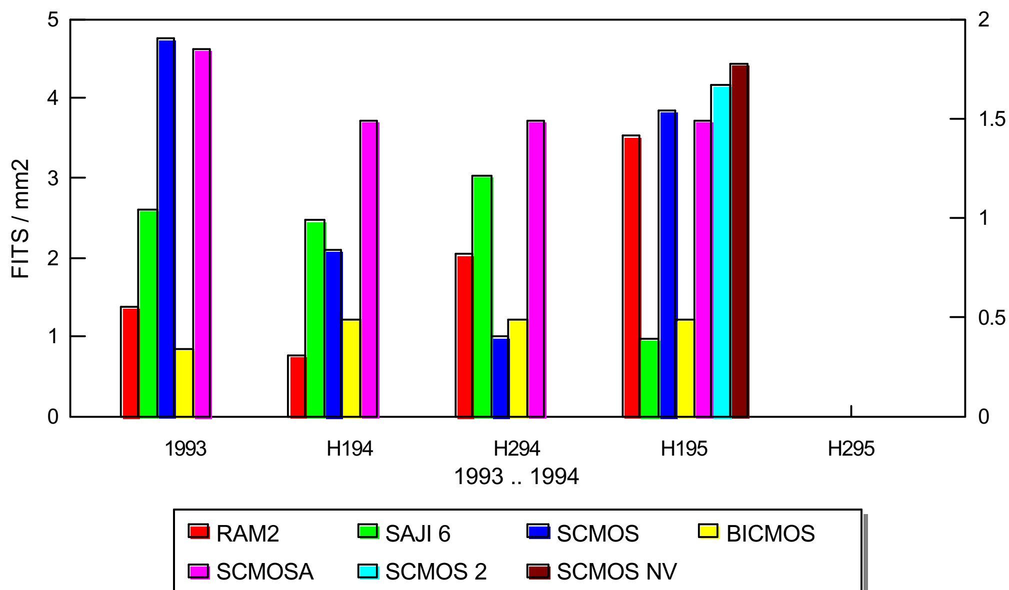




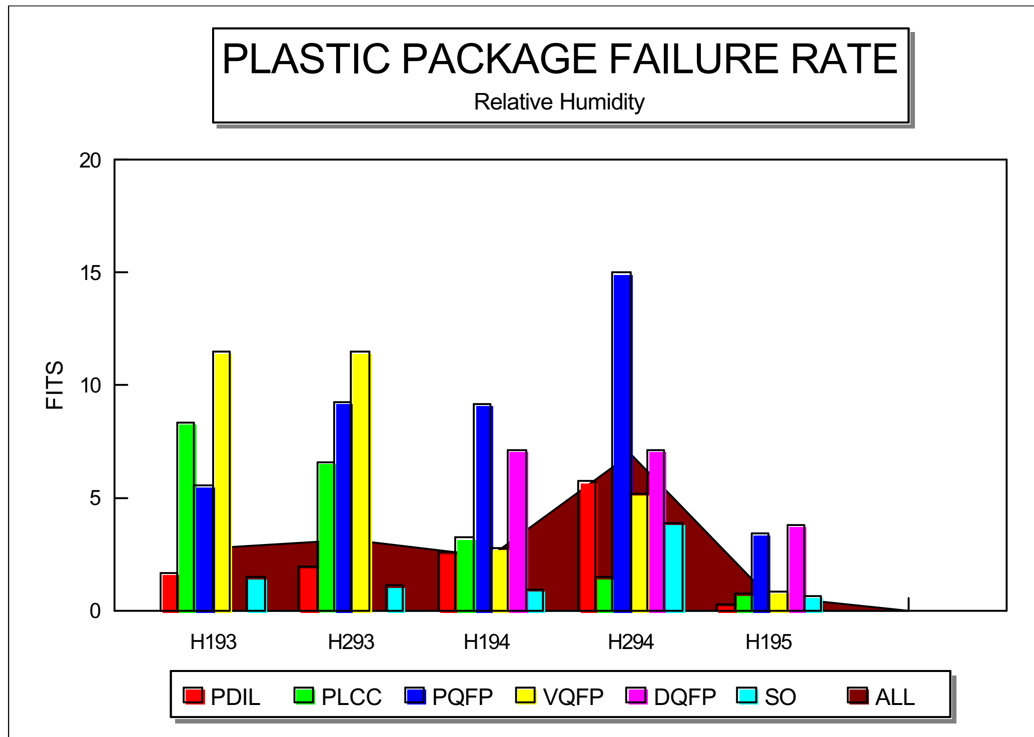


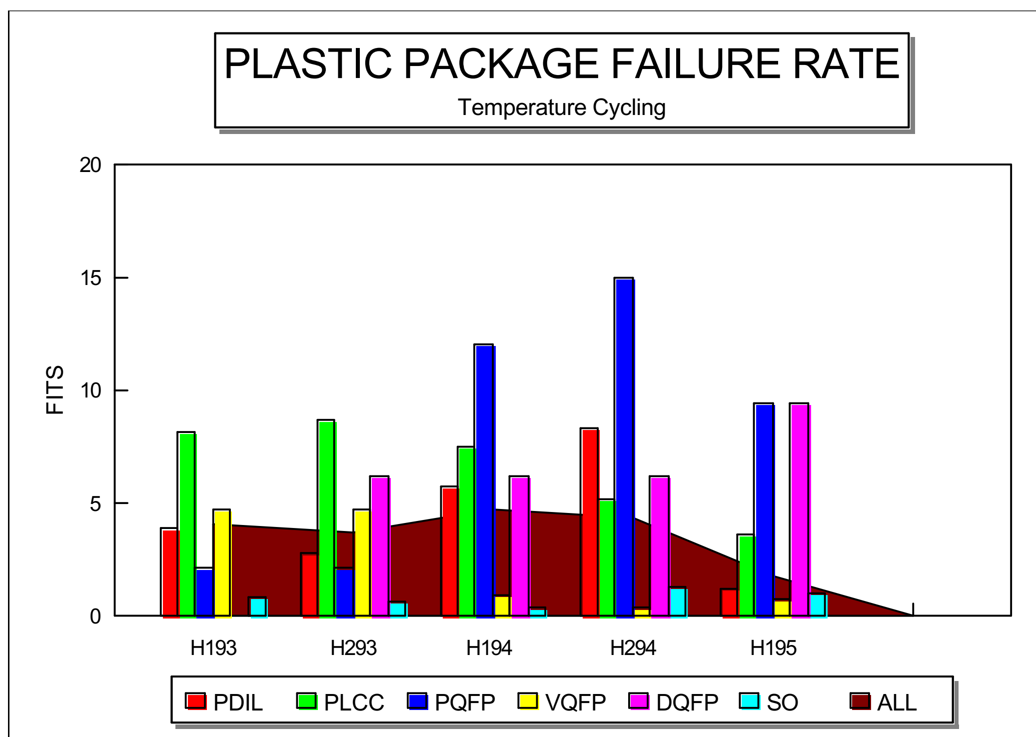
Global Reliability Data (cont'd)





Global Reliability Data (cont'd





2.2 Reliability Data per Process

2.2.1 Data for process : RAM 2

Early Failure Rate

Sample size	21, 696 parts
Average Tested Die Surface	29.49 mm2
Early Failure Rate	415 ppm
EFR / mm2	14.07 ppm / mm2

Latent Failure Rate

Cumulated Test Hours	1, 728, 548 hours
Equivalent Device Hours	$1.4\ 10^{8}$ hours
Average Tested Die Surface	26.99 mm2
Latent Failure Rate	38.15 fits
LFR / mm2	1.41 fit / mm2

LFR given with 60% CL and calculated with Ta = 55°C and Ea = 0.6 eV.

The measurement results of the Early Failure rate and of the Latent Failure rate are affected by the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

2.2.2 Data for process : SAJI 6

Early Failure Rate

Sample size	48,455 parts
Average Tested Die Surface	29.55 mm2
Early Failure Rate	1, 093 ppm
EFR / mm2	37.01 ppm / mm2

Latent Failure Rate

Cumulated Test Hours	2, 317, 464 hours
Equivalent Device Hours	$1.8\ 10^8$ hours
Average Tested Die Surface	28.1 mm2
Latent Failure Rate	10.9 fits
LFR / mm2	0.39 fit / mm2

LFR given with 60% CL and calculated with Ta = 55°C and Ea = 0.6 eV.

The measurement results of the Early Failure rate and of the Latent Failure rate are affected by the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

2.2.3 Data for process : SCMOS 1/2

Early Failure Rate

Sample size	90, 236 parts
Average Tested Die Surface	26.3 mm2
Early Failure Rate	520 ppm
EFR / mm2	19.8 ppm / mm2

Latent Failure Rate

Cumulated Test Hours	4, 978, 868 hours
Equivalent Device Hours	3.9 10^8 hours
Average Tested Die Surface	27.7 mm2
Latent Failure Rate	42.5 fits
LFR / mm2	1.54 fit / mm2

LFR given with 60% CL and calculated with Ta = 55°C and Ea = 0.6 eV.

The measurement results of the Early Failure rate and of the Latent Failure rate are affected by the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

2.2.4 Data for process : SCMOS 2

Early Failure Rate

Sample size	584 parts
Average Tested Die Surface	43.46 mm2
Early Failure Rate	6849 ppm
EFR / mm2	157.6 ppm / mm2

Latent Failure Rate

Cumulated Test Hours	481, 012 hours
Equivalent Device Hours	37, 928, 329 hours
Average Tested Die Surface	46.78 mm2
Latent Failure Rate	195 fits
LFR / mm2	4.17 fit / mm2

LFR given with 60% CL and calculated with Ta = 55°C and Ea = 0.6 eV.

The measurement results of the Early Failure rate and of the Latent Failure rate are affected by the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

2.2.5 Data for process : SCMOS NV

Early Failure Rate

Sample size	518 parts
Average Tested Die Surface	68.8 mm2
Early Failure Rate	0 ppm
EFR / mm2	0 ppm / mm2

Latent Failure Rate

Cumulated Test Hours	38, 000 hours
Equivalent Device Hours	29, 963, 342 hours
Average Tested Die Surface	68.8 mm2
Latent Failure Rate	303 fits
LFR / mm2	4.43 fit / mm2

LFR given with 60% CL and calculated with Ta = 55°C and Ea = 0.6 eV.

The measurement results of the Early Failure rate and of the Latent Failure rate are affected by the die size of the products choosen for the tests.

Therefore, so as to eliminate this influence, and as the failure modes observed during these tests are strongly related to the processing defect density, the Early Failure and Latent Failure rates are rated to the average tested surface.

This will allow for every product to calculate the relevant EFR and LFR as shown in the Product Index.

2.3 Reliability Data per Packages

2.3.1 Data for Plastic Packages

Package	Test	Sample Size	Equivalent Hours	Rejects	Fits
PDIL	Rel. Humidity	1, 388	$3.15\ 10^{9}$	1	0,3
	Temp. Cycling	1, 191	$2.41\ 10^{9}$	3	1,2
PLCC	Rel. Humidity	2, 201	$4.1\ 10^{9}$	3	0,7
	Temp. Cycling	1, 568	$3.4\ 10^{9}$	12	3,6
PQFP	Rel. Humidity	180	$2.94\ 10^{8}$	1	3,4
	Temp. Cycling	90	$1.07\ 10^{8}$	0	<9.4n/s
TQFP	Rel. Humidity	190	$4.89\ 10^{8}$	0	<2
	Temp. Cycling	90	$2.14\ 10^{8}$	0	<4.7
VQFP	Rel. Humidity	925	$3.75\ 10^{9}$	3	0,8
	Temp. Cycling	692	$1.42\ 10^{9}$	0	<0.7
DQFP	Rel. Humidity	195	$2.65\ 10^{8}$	0	<3.8
	Temp. Cycling	45	$1.7\ 10^{8}$	0	<9.4n/s
SO..	Rel. Humidity	887	$1.6\ 10^{9}$	1	0,6
	Temp. Cycling	495	$1.01\ 10^{9}$	0	<1

n/s: result not significant - number of tested parts too low.

Data presented in the topic Relative Humidity are issued either from the test 85°C / 85% RH / 5.5V biased or from the HAST test at 130°C / 85% RH / 5.5V biased as described in the chapter 4.

As previously decribed, the failure rates are calculated for a product life in the commercial temperature range 0 - 70°C, assuming 3 temperature cycles per day, and 30°C - 60% RH average ambiant conditions.

2.3.2 Data for Hermetic Packages

Package		D1	D2	D3	D4	D5	D6	D7	D8
CDIL	Qty	360	66	531	590	337	75	54	163
	Rej.	0	0	0	10°	0	0	0	0
MLLC	Qty								
	Rej.	0	0	0	0	0	0	0	0
MLCC	Qty								
	Rej.	0	0	0	0	0	0	0	0
SB	Qty								
	Rej.	0	0	0	0	0	0	0	0
PGA	Qty								
	Rej.	0	0	0	0	0	0	0	0
MQFP	Qty								
	Rej.	0	0	0	0	0	0	0	0
MFP	Qty								
	Rej.	0	0	0	0	0	0	0	0
CQP..	Qty	60	9	75	78	45	12	9	15
	Rej.	0	0	0	0	0	0	0	0

n/a: test not applicable to this product family.

(°): NO REJECT IN MIL-STD 38510 COMPLIANT PRODUCTS

The reliability tests on hermetic packages are made in accordance to the MIL883 test methods whatever is the range of the product, MIL STD 38510 compliant or not.

The tests are named in accordance to the method 5005.

2.4 Main Failure Modes and Improvements

2.4.1 Die or Silicon Related Failures

Main Failure Modes	Improvements
Metal bridging / particules	New etching & cleaning equipments Automatic inspection of metal layers.
Metal stringers	Upgrade of concerned mask sets.
Contact spiking / Rocks	Upgrade of concerned mask sets.
Poly particles Poly degradation	New deposition & cleaning equipments Automatic inspection of poly layers.
Interlayer oxide defects	New cleaning equipments.
Gate oxide pinholes	New cleaning process under evaluation 2nd half 95..

2.4.2 Package or Assembling Related Failures

Main Failure Modes	Improvements
Passivation defects Limited to old mask set 80C51, 80C52.	Mask sets obsoleted. New generation generalized in early 95. Molding process parameters optimized.
Bond lifted limited to PLCC44, SO	New set of bonding process parameters. Evaluation of new pad cleaning. in 2nd half 95.
Sealing glass crack	Sealing process parameters revised.

3 Product Index

Device	Technology	Function	EFR (ppm)	LFR (fits)
AFGGXX	SAJI	ASIC-CUSTOM	5 474	58
AFGOXX	SCMOS	ASIC-CUSTOM	1 386	108
850	SAJI	ASIC-MB SERIES	603	6
5 000	SAJI	ASIC-MB SERIES	2 332	25
6 500	SAJI	ASIC-MB SERIES	2 832	30
6 600	SAJI	ASIC-MB SERIES	2 898	30
7 500	SAJI	ASIC-MB SERIES	3 213	34
MC05K	SCMOS	ASIC-MC SERIES	515	40
MC10K	SCMOS	ASIC-MC SERIES	881	68
MC22K	SCMOS	ASIC-MC SERIES	1 224	95
MC35K	SCMOS	ASIC-MC SERIES	1 895	147
MC50K	SCMOS	ASIC-MC SERIES	2 537	197
MCT02K	SCMOS	ASIC-MC SERIES	273	21
MCT08K	SCMOS	ASIC-MC SERIES	687	53
MCT12K	SCMOS	ASIC-MC SERIES	1 018	79
MCT29K	SCMOS	ASIC-MC SERIES	1 545	120
MCT66K	SCMOS	ASIC-MC SERIES	3 129	243
MF05K	BICMOS	ASIC-MF SERIES	154	7
MF13K	BICMOS	ASIC-MF SERIES	269	12
MF32K	BICMOS	ASIC-MF SERIES	454	20
AFKUXX	SCMOS 2	ASIC-STANDARD CELLS	1 747	136
AFTOXX	SCMOS	DATACOM-29C461B VAN CONTROLLER	222	17
CN20AP	SAJI	DATACOM-HERMES	566	6
29C95	SCMOS	DATACOM-NETWORK-ECMA CONTROLLER	1 756	136
29C94	SCMOS	DATACOM-NETWORK-HDLC CONTROLLER	1 756	136
29C93A	SCMOS	DATACOM-NETWORK-T.R.A.C.	687	53
29C921	SCMOS	DATACOM-NETWORK-X21 CONTROLLER	279	22
29C80	SCMOS	DATACOM-VIDEO-DCT	566	44
29C84	SCMOSA	DATACOM-VIDEO-DECODER	0	0
29C82	SCMOS	DATACOM-VIDEO-JPEG DECODER	1 836	142
3 057	SAJI	DATACOM-VOICE COMBO	792	8
67 130	SCMOS	DPRAM-1K*8	341	26
67 140	SCMOS	DPRAM-1K*8	341	26
67 132	SCMOS	DPRAM-2K*8	442	34
67 142	SCMOS	DPRAM-2K*8	442	34
67 024	SCMOS	DPRAM-4K*16	1 044	81
67024E	SCMOS	DPRAM-4K*16	1 044	81
67 005	SCMOS	DPRAM-8K*8	1 103	86
67 201	SCMOS	FIFO-0.5K*9	261	20
67201A	SCMOS	FIFO-0.5K*9	261	20
67 202	SCMOS	FIFO-1K*9	261	20
67202A	SCMOS	FIFO-1K*9	261	20
67202E	SCMOS	FIFO-1K*9-RT	261	20
67 203	SCMOS	FIFO-2K*9	505	39
67 204	SCMOS	FIFO-4K*9	505	39
67 205	SCMOS	FIFO-8K-9	802	62

Device	Technology	Function	EFR (ppm)	LFR (fits)
67205E	SCMOS	FIFO-8K*9 RT	802	62
80C51	SAJI	MICRO-RAM 128-ROM 4K	929	10
80C51	SCMOS	MICRO-RAM 128-ROM 4K	327	25
80C31	SCMOS	MICRO-RAM 128-ROMLESS	327	25
83C154	SAJI	MICRO-RAM 256-ROM 16K	1 210	13
83C154	SCMOS	MICRO-RAM 256-ROM 16K	428	33
83C154D	SCMOS	MICRO-RAM 256-ROM 32K	570	44
83C154D	SAJI	MICRO-RAM 256-ROM 32K	1 625	17
80C52	SAJI	MICRO-RAM 256-ROM 8K	1 210	13
80C52	SCMOS	MICRO-RAM 256-ROM 8K	521	40
80C32	SCMOS	MICRO-RAM 256-ROMLESS	327	25
80C32	SAJI	MICRO-RAM 256-ROMLESS	1 210	13
83C154	SCMOS	MICRO-RAM 256-ROMLESS	428	33
83C154	SAJI	MICRO-RAM 256-ROMLESS	1 210	13
65 262	SAJI	SRAM-16K*1	844	9
65767B	RAM2	SRAM-16K*1	146	15
65688A	SCMOS	SRAM-16K*4	471	37
65 788	RAM2	SRAM-16K*4	269	27
65 888	BICMOS	SRAM-16K*4	179	8
65 789	RAM2	SRAM-16K*4 with OE	269	27
65 889	BICMOS	SRAM-16K*4 with OE	179	8
65 790	RAM2	SRAM-16K*4 with sep. IO	269	27
65 791	RAM2	SRAM-16K*4 with sep. IO & Transp. W	269	27
65 697	SCMOS	SRAM-256K*1	1 289	100
65 797	RAM2	SRAM-256K*1	577	58
65 162	SAJI	SRAM-2K*8	844	9
65728B	RAM2	SRAM-2K*8	146	15
65 656	SCMOS	SRAM-32K*8	1 289	100
65656E	SCMOS	SRAM-32K*8	1 289	100
65 756	RAM2	SRAM-32K*8	577	58
65 687	SCMOS	SRAM-4K*1	469	36
65687A	SCMOS	SRAM-4K*1	471	37
65768B	RAM2	SRAM-4K*4	146	15
65 787	RAM2	SRAM-64K*1	269	27
65 698	SCMOS	SRAM-64K*4	1 289	100
65 798	RAM2	SRAM-64K*4	577	58
65 799	RAM2	SRAM-64K*4 with OE	577	58
65 795	RAM2	SRAM-64K*4 with sep. IO	577	58
65 796	RAM2	SRAM-64K*4 with sep. IO & transp. W	577	58

4 Reliability Test Descriptions

4.1 Early Failure Rate (EFR) measurement:

The devices are submitted to a dynamic life test for 12 hours at 150°C and V_{cc}=5.75V.

4.2 Latent Failure Rate (LFR) measurement - High Temp. Operating Life Test

The devices are submitted to a dynamic life test for up to 1000 hours at 150°C and V_{cc}=5.75V.

4.3 Latent Failure Rate (LFR) measurement - High Temp. Static Life Test

The devices are submitted to a static life test for up to 1000 hours at 150°C and V_{cc}=5.75V.

4.4 Environmental tests (as referenced in the detailed list)

Temperature cycles:	T/C1	-65 / + 150°C - air / air - 15' dwell time - 10, 500 & 1000 cycles.
Thermal shocks:	T/C2	-65 / + 150°C - liquide / liquide - 15' dwell time - 15 cycles.
Mositure resistance:	HU01	85°C / 85% RH - 5.5V static bias - 500 & 1000 hrs.
	HU02	85°C / 85% RH - no bias - 500 & 1000 hrs.
	HA01	130°C / 85% RH / 1.7 atm. - 5.5V static bias - 168 hrs
	HA02	130°C / 85% RH / 1.7 atm. - no bias - 168 hrs
	PCT1	121°C / 100%RH / 1.2 atm. - no bias - 168 hrs
Preconditionning & endurance:	ENI1/ENIR	85/85-168hrs storage + IR soldering + T/C2 + HA02
	ENI2	IR soldering + T/C2 + HA02
	ENV1	85/85-168hrs storage + dip soldering (Trough hole) + T/C2 + HA02
	ENV2	Dip soldering (Trough hole) + T/C2 + HA02
	ENH1	85/85-168hrs storage + dip soldering (Trough hole) + HU01
	ENH2	dip soldering (Trough hole) + HU01
	ENH3	85/85-168hrs storage + IR soldering + HU01
	ENH4	IR soldering + HU01
	ETC1	85/85-168hrs storage + dip soldering (Trough hole)+ T/C1
	ETC2	dip soldering (Trough hole)+ T/C1
	ETC3	85/85-168hrs storage + IR soldering + T/C1
	ETC4	IR soldering + T/C1
	ENA1	85/85-168hrs storage + IR soldering + T/C1-10 cycles + HA01-500hrs
	ENP1	85/85-168hrs storage + IR soldering + T/C1-10 cycles + PCT1 -500hrs

Common to all preconditionning & endurance tests:

Initial drying 125°C / 24 hrs.
IR soldering done acc. to MHS pofile with T_{max}=240°C - 30 sec. over 220°C. The JEDEC profile with T_{max}=230°C - 1 min. over 220°C done twice is under introduction (2nd half 95).
Dip soldering done at 250°C - 10 sec.
Electrical test & visual inspection after solderings (CSAM may be included)
Final electrical test after endurance tests

5 Technology Descriptions -- Typical values

5.1 Technology Description : RAM 2

Name	Z83
Technology	CMOS
Product families	SRAMs 4 transistors cells and ULCs
Wafer size	6 inches (150 mm)
Wafer thickness (final)	470 µm
Number of masks	16 (SRAMs) 10 (ULCs)
Number of poly layers	2 (SRAMs) 1 (ULCs)
Poly 1 thickness	3000 A
Poly width	0.8 µm
Poly spacing	1.9 µm
Poly 2 thickness	1500 A
Contact size	1.2 µm
Number of metal layers	2
Metal 1 material	AlSi / Ti
Metal1 thickness	8950 A
Metal 1 width	1.3 µm
Metal 1 spacing	1.3 µm
Metal 2 material	AlSi/Ti
Metal 2 thickness	10500 A
Metal 2 width	2.2 µm
Metal 2 spacing	1.8 µm
Via size	1.6 µm
Gate material	Polysilicide
Gate dielectric material	Silicon dioxide
Effectice channel length	0.8 µm
Gate Oxide thickness	195 A
Glassivation material	SiOxNy on SiO2
Thickness	18000 A

5.2 Technology Description : SAJI 6

Name	Z63
Technology	CMOS
Product families	Microcontrollers, Memories and Asics
	6 inches (150 mm)
Wafer thickness (final)	470 µm
Number of masks	9
Number of poly layers	1
Poly 1 thickness	5000 A
Poly width	1.6 µm
Poly spacing	2.0 µm
Number of metal layers	1
Metal 1 material	AlSi
Metal1 thickness	10000 A
Metal width	3 µm
Metal spacing	2 µm
Contact size	1.4 µm
Gate material	Polysilicide
Gate dielectric material	Silicon dioxide
Effective channel length	1.6 µm
Min gate Oxide thickness	305 A
Glassivation material	SiOxNy on SiO2
Thickness	18000 A

5.3 Technology Description : SCMOS

Name	Z86
Technology	CMOS
Product families	SRAMs, Micros, Datacoms and Asics
Substrate type	Epi or bulk (Micros)
Wafer size	6 inches (150 mm)
Wafer thickness (final)	470 µm
Number of masks	13 (SRAMs, Asics & Datacom) 11 (Micros)
Number of poly layers	1
Poly 1 thickness	3000 A
Poly width	0.8 µm
Poly spacing	2.0 µm
Number of metal layers	2 (1 for Micros)
Metal 1 material	W / Ti
Metal1 thickness	5500 A
Metal 2 material	AlSi / Ti
Metal2 thickness	10500 A
Metal width	1.3 µm (M1), 1.6 µm (M2)
Metal spacing	1.5 µm (M1), 1.6 µm (M2)
Contact size	1.2 µm
Via size	1.3 µm
Gate material	Polysilicide
Gate oxide material	Silicon dioxide
Effective channel length	0.8 µm
Gate oxide thickness	195 A
Glassivation material	SiOxNy on SiO2
Thickness	18000 A

5.4 Technology Description : SCMOS 2

Name	Z91
Technology	CMOS
Product families	Asics - Memories
Substrate type	Epi
Wafer size	6 inches (150 mm)
Wafer thickness (final)	470 µm
Number of masks	13 max
Number of poly layers	1
Poly thickness	3500 A
Poly width	0.6 µm
Poly spacing	0.75 µm
Number of metal layers	3 (Asics) 2 (Memories)
Metal 1 material	AlSi / Ti
Metal 1 thickness	7700 A
Metal 2 material	AlSi / Ti
Metal 2 thickness	7700 A
Metal 3 (2) material	AlSi / Ti
Metal 3 (2) thickness	10500 A
Metal width	0.8 µm (M1), 0.9 µm (M2),1.0 µm (M3/2)
Metal spacing	0.95 µm (M1), 1.2 µm (M2), 1.3 µm (M3/2)
Contact size	0.8 µm
Via size	0.7 µm (M1/M2), 0.8 µm (M2/M3)
Gate material	Polysilicide
Gate dielectric material	Silicon dioxide
Effective channel length	0.6 µm
Gate oxide thickness	145 A
Glassivation material	SiOxNy on SiO2
Thickness	18000 A

5.5 Technology Description : SCMOS NV

Name	Z89
Technology	CMOS
Product families	embedded EPROM, E2PROM, FLASH
Substrate type	Epi or bulk depending on end poduct
Wafer size	6 inches (150 mm)
Wafer thickness (final)	470 µm
Number of masks	21 max (2 Metal, EPROM & FLASH)
Core Poly thickness	3000 A
Core Poly width	0.8 µm
Number of metal layers	2
Metal 1 material	AlSi / Ti
Metal1 thickness	8000 A
Metal 2 material	AlSi / Ti
Metal2 thickness	10500 A
Metal width	1.3 µm (M1), 1.6 µm (M2)
Metal spacing	1.5 µm (M1), 1.6 µm (M2)
Contact size	1.2 µm
Via size	1.4 µm
Gate material	Polysilicide
Gate dielectric material	Silicon dioxide
Effective channel length	0.87 µm (NMOS), 0.82 µm (PMOS)
MOS gate oxide thickness	195 A
FAMOS gate Ox. thickness	225 A
Tunnel Ox. thickness	80 A
Glassivation material	SiOxNy on SiO2
Thickness	18000 A

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